Rudrajit Datta

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RESEARCH INTERESTS

Designing novel error correction codes for semiconductor memories, cache debug & diagnosis, DFT, VLSI design, VLSI testing, CAD for fault tolerance.

EDUCATION

The University of Texas at Austin
Ph.D., Electrical and Computer Engineering, 2011
Advised by Prof. Nur Touba.

MS, Electrical and Computer Engineering, 2009

Indian Institute of Technology, Kharagpur
B.Tech, Electrical Engineering. 2007

WORK EXPERIENCE

Intel Corporation
January '12 – Present, Software Engineer, Debug and Diagnosis Solutions, Hillsboro:
Exploring CAD solutions leading to fault isolation and failure analysis of factors affecting yield on latest technological nodes, with primary focus on memory caches.

May '11 – August, '11, Graduate Intern, Debug and Diagnosis Solutions Team, Hillsboro:
Worked on large signal array diagnosis. Helped develop a tool that would generate layout level information for failed memory cells, thereby aiding in memory diagnosis.

June '09 - August '10, Graduate Intern, System Validation Full Chip - Power Management/DFx, Atom Validation & Emulation Group, Austin:
Performed post-silicon validation of power state flows and low-power DFx features for next generation LPIA (Low Power Intel Architecture) microprocessors and SoCs.

June '08 - August '08, Graduate Intern, SoC Enabling Group - DFx Architecture, Hillsboro:
Worked on developing and integrating the SoC trigger engine, developed as an IP-block and implemented in System Verilog, would combine triggers from different parts of the system using Boolean functions to generate a global trigger.
Awarded MG (Mobility Group) Kudos for work done during internship.

The University of Texas at Austin, Teaching Assistant,
EE319K – Introduction to Embedded Systems, Fall 2007 & Spring 2008.
EE382M – Dependable Computing, Spring 2011
EE382M – VLSI Testing, Fall 2011

Goldman Sachs
May '06 - July '06, Summer Analyst, Proprietary Accounting and Risk Analysis (PARA), Bangalore:
Helped automate the testing environment in PARA for checking in latest code base into production; streamlining entire testing process.

PUBLICATIONS

[1] R. Datta, N. A. Touba, "Exploiting Unused Spare Columns to Improve Memory ECC", *Proc. of IEEE VLSI Test Symposium*, pp. 47-52, May 2009. [pdf]

[2] R. Datta, N. A. Touba, "Post-Manufacturing ECC Customization Based on Orthogonal Latin Square Codes and Its Application to Ultra-Low Power Caches", *Proc. of IEEE International Test Conference*, November 2010. [pdf]

[3] R. Datta, N. A. Touba, "Designing a Fast and Adaptive Error Correction Scheme for Increasing the Lifetime of Phase Change Memories", *Proc. of IEEE VLSI Test Symposium 2011*, pp. 134-139, May 2011. [pdf]

[4] R. Datta, N. A. Touba, "X-Stacking – A Method for Reducing Control Data for Output Compaction", *Proc. of IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems*, pp. 332-338, October 2011. [pdf]

[5] R. Datta, N. A. Touba, "Generating Burst-error Correcting Codes from Orthogonal Latin Square Codes – a Graph Theoretic Approach", *Proc. of IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems*, pp. 367-373, October 2011. [pdf]
(Received Best Student Award)

[6] J.-S. Yang, R. Datta, "Efficient Function Mapping in Nanoscale Crossbar Architecture", *Proc. of IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems*, pp. 190-196, October 2011. [pdf]

[7] R. Datta, "Adaptable and Enhanced Error Correction Codes for Efficient Error and Defect Tolerance in Memories", Ph.D. Dissertation, The University of Texas at Austin, December 2011. [pdf]

OTHER PROJECTS

Implemented a 3-value fault simulator: The fault simulator implemented parallel pattern single fault (PPSF) algorithm and was developed in C.

Implementing various algorithms in context of computational finance: Design points varied from usage of efficient data structures viz. hash tables, binary search trees (BSTs) to approximation algorithms, heuristics etc. Java was the programming language used.

SKILLS

Programming languages: C, Java, Perl, Tcl, HTML
Hardware description language: Verilog, SystemVerilog
Application Software: HSPICE, Primetime

COURSEWORK

Computer Architecture, VLSI Testing, Dependable Computing, VLSI I, VLSI II, Algorithms, Formal Semantics & Verification, Optimization Issues in VLSI CAD, VLSI Physical Design Automation, Nanometer Scale IC Design, High Speed Computer Arithmetic, Embedded System Design and Modeling.

ACCOMPLISHMENTS

Jointly awarded **Best Student Presentation** at International Test Synthesis Workshop, 2009.

Within top 1% of the graduating class at the Indian Institute of Technology, Kharagpur.

Student member of IEEE.

Governor of Dramatics Society at IIT Kharagpur.

REFERENCES

Available upon request.